AMENDMENTS TO THE SPECIFICATION

The paragraph beginning at page 3, line 5 has been amended as follows:

It is advantageous to form integrated circuits with smaller individual elements so that as many elements as possible may be formed in a single chip. In this way, electronic equipment becomes smaller, assembly and packaging costs are minimized, and integrated circuit performance is improved. The capacitor is usually the largest element of the integrated circuit chip. Consequently, the development of smaller DRAMs focuses to a large ~~extend~~ extent on the capacitor. Three basic types of capacitors are used in DRAMs -- planar capacitors, trench capacitors, and stacked capacitors. Most large capacity DRAMs use stacked capacitors because of their greater capacitance, reliability, and ease of formation. For stacked capacitors, the side of the capacitor connected to the transistor is commonly referred to as the "storage node", and the side of the capacitor connected to the reference voltage is called the cell plate. The cell plate is a layer that covers the entire top array of all the substrate-connected devices, while there is an individual storage node for each respective storage bit site.

The paragraph beginning at page 9, line 12 has been amended as follows:

Referring to Figure 3, a storage plate 40 is deposited. Storage plate 40, which is substantially composed of an electrically conductive material, is preferably composed of doped polysilicon or doped rough textured polysilicon. Referring to Figure 4, storage plate 40 has been subjected to ~~an~~ a planarizing process, such as chemical mechanical polishing, to form a storage node layer 42.

The paragraph beginning at page 10, line 9 has been amended as follows:

Referring to Figure 7, there is illustrated a first etch step wherein a photoresist layer 60 is spun on, exposed, and selectively removed during development to expose a preferred bit line contact site. The first etch step etches cell plate layer 46 and may involve the use of an isotropic component, resulting in an undercut into cell plate layer 46

~~capacitor cell dielectric layer 44~~. The first etch step penetrates the noted conductive and insulative layers and partially penetrates into lower bulk insulator layer 36. The first step, however, will preferably be anisotropic so as to form a contact hole 70 with no undercut into cell plate layer 46 or less than is illustrated in Figure 7. Similar to that which is illustrated in Figure 11 as an anisotropic etch extending through layers 36, 44, 46, and 48, it is preferable that an anisotropic etch be performed through layers 36, 44, 46, and 48 seen in Figure 7 so as to form straight side walls of the etched contact hole 70. The etch process through layers 36, 44, 46, and 48 seen in Figure 7, however, can be performed so as to have an isotropic component so as to leave contact hole 70 without straight side walls, although such an isotropic etch is not preferred.

The paragraph beginning at page 11, line 24 has been amended as follows:

Figure 10 illustrates an example of a second embodiment of the present invention. Cell plate layer 46 maximizes its capacitative effect upon storage node layer 42 by its being wrapped conformally around two opposing vertical faces of storage node layer 42. In this embodiment, the cell-to-cell bridging of cell plate layer 46 is deeper in the structure. A primary insulator layer 48 is deposited upon an upper bulk insulator layer 51. Then, a partial etch is made through primary insulator layer 48 into upper bulk insulator layer 51 and stopping within a lower bulk insulator layer 36 so as to form a contact hole 70. A secondary sleeve insulator layer 50 is then deposited upon primary insulator layer 48 and within contact hole 70. An anisotropic etch removes secondary sleeve insulator layer 50 from the bottom of contact hole 70 and other laterally exposed portions thereof. The anisotropic etch stops on insulator layer 48, leaving secondary sleeve insulator layer 50 as a liner on the sidewalls of contact hole 70. A subsequent ~~openings~~ opening can be formed to provide a contact to active region 18B and a contact plug is formed through secondary sleeve insulator layer 50 and in contact with active region 18b.

The paragraph beginning at page 12, line 11 has been amended as follows:

Figure 11 illustrates a third embodiment of the present invention in which a cell plate structure is like the second embodiment, but also has a cell plate insulating layer 48 disposed on top of cell plate layer 46. The upper surface of cell plate layer 46 is partially insulated by cell plate insulating layer 48. This third embodiment may be preferred where a neighboring site requires cell plate insulating layer 48, such as where cell plate insulating layer 48 is useful or convenient so as to avoid masking for deposition of cell plate insulating layer 48. Cell plate insulating layer 48 should be composed of a material different from capacitor cell dielectric layer 44 so as to best facilitate the partial etch into lower bulk insulator layer 36. A primary insulator layer 49 is deposited upon an [[a]] upper bulk insulator layer 51. Then, a partial etch is made through primary insulator layer 49 into upper bulk insulator layer 51 and stopping within [[a]] lower bulk insulator layer 36 so as to form a contact hole 70. A secondary sleeve insulator layer 50 is then deposited upon primary insulator layer 49 and within contact hole 70. An anisotropic etch removes secondary sleeve insulator layer 50 from the bottom of contact hole 70 and other laterally exposed portions thereof. The anisotropic etch stops on primary insulator layer 49, leaving secondary sleeve insulator layer 50 as a liner on the sidewalls of contact hole 70.

The paragraph beginning at page 13, line 6 has been amended as follows:

Figures 12-14 illustrate the function of the first embodiment of the present invention as it provides a self-aligning contact hole site for further processing. Referring to Figures 12-14, there are illustrated qualitative process flow examples of ~~which~~ both proper alignment and misalignment in the formation of a contact plug in a contact hole. The misalignment example is set forth to illustrate the self alignment feature of the invention.

The paragraph beginning at page 13, line 24 has been amended as follows:

Figure 13 shows that an upper bulk insulator layer 51 is deposited within the area defined by sleeve insulator layer 50 and upon cell plate insulating layer 48. A patterned

photoresist layer 56 has been formed upon upper bulk insulator layer 51. The pattern in patterned photoresist layer 56 is intended to be aligned with respect to sleeve insulator layer 50 so that a subsequent etch will open a contact through upper bulk insulator layer 51 and lower bulk insulator layer 36 to expose a contact on active area 18b. Patterned photoresist layer 56, however, ~~maybe~~ <u>may be</u> misaligned with respect to sleeve insulator layer 50, as was illustrated by the foregoing discussion of Figure 12.

The paragraph beginning at page 14, line 14 has been amended as follows:

Referring to Figure 14, a circle 80 illustrates in phantom a cross-section of an etch hole through upper bulk insulator layer 51. A center line 81 represents an axis passing through the center of circle 80. In Figure 14, center line 71 represents the axis passing through the center of sleeve insulator layer 50. The symbol Δ_3 ~~represent~~ <u>represents</u> the misalignment from the center of circle 80 to the center of sleeve insulator layer 50.

The paragraph beginning at page 16, line 1 has been amended as follows:

Figure 16 shows the divergent types of contacts that can be made using the invention, although all of the depicted contacts need not be present in the same structure nor be situated as depicted in Figure 16. In Figure 16, circle 90 illustrates in phantom a cross-section of an etch hole, made by conventional etch processes, through upper bulk insulator layer 51. A contact plug 72 [[in]] <u>is</u> upon source/drain region 18b. Electrically conductive bit line contact 92 is situated within contact hole 70 and passes through sleeve insulator layer 50 to terminate upon contact plug 72. Circle 94 illustrates in phantom a cross-section of a contact hole 98, made by conventional etch processes, through upper bulk insulator layer 51 and into a transistor so as to stop on a gate electrode 24 beneath an insulating protective layer 28 of a transistor. Electrically conductive contact 100 is situated within contact hole 98 and passes through a sleeve insulator layer 52 to make contact with gate 24. Circle 104 illustrates in phantom a cross-section of a contact hole 106, made by conventional etch processes, through upper bulk insulator layer 51 and into storage node layer 42. Electrically conductive contact 102 is situated within contact hole 106 and passes through a sleeve insulator layer 53 to make contact with storage node

layer 42. Sleeve insulator layer 53 insulates electrically conductive contact 102 from cell plate layer 46.

AMENDMENTS TO THE CLAIMS

1. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer thereupon~~, a dielectric layer upon the lower bulk insulator layer, and a conductor layer upon the dielectric layer~~;

forming a dielectric layer on the lower bulk insulator layer;

forming a conductor layer upon the dielectric layer;

forming a first insulator layer upon the conductor layer;

forming a second insulator layer upon the first insulator layer, said second insulator layer having a top surface ~~and having a thickness greater than that of the first insulator layer~~;

selectively removing the first and second insulator layers so as to form [[a]] <u>an</u> opening defined by the lower bulk insulator layer, the dielectric layer, the conductor layer, and the first and second insulator layers, the opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

forming a sleeve insulator layer ~~upon~~ <u>over</u> the top surface of said second insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the dielectric layer, the conductor layer, and the first and second insulator layers;

removing the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate, <u>and</u> from the top surface of the second insulator layer, such that the sleeve insulator layer has a terminus ~~at an interface between the first and second insulator layers~~ <u>adjacent to the top surface of the second insulator layer</u>, and extends to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the dielectric layer; and

removing material of the lower bulk insulator layer to expose a contact on the semiconductor substrate.

2. (original) A method according to Claim 1, wherein at least one of removing the sleeve insulator layer and removing material of the lower bulk insulator layer comprises etching.

3. (original) A method according to Claim 1, further comprising forming a conductive structure in contact with each of the sleeve insulator layer, the contact on the semiconductor substrate, and a sidewall of the lower bulk insulator layer that is situated in between the contact on the semiconductor substrate and the sleeve insulator layer.

4. (original) A method according to Claim 3, wherein the conductive structure has an end comprising at least one refractory metal silicide, said end of said conductive structure being situated upon the contact on the semiconductor substrate.

5. (original) A method according to Claim 3, wherein the conductive structure comprises at least one material selected from the group consisting of tungsten, titanium/titanium nitride/tungsten, titanium/tungsten, aluminum, copper, a refractory metal silicide with aluminum, and a refractory metal silicide with copper.

6. (currently amended) A method according to ~~as defined in~~ Claim 1, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4.

7. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a capacitor storage node thereon and having an active region therein that is adjacent to a transistor on said semiconductor substrate, and further having a lower bulk insulator layer upon the active area, the transistor, and the semiconductor substrate, a capacitor dielectric layer upon the lower bulk insulator layer and upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer, said upper bulk insulator layer having a top surface and a thickness that is greater than that of the cell plate insulator layer;

etching [[a]] an opening defined by the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, the cell plate insulator layer, and the upper bulk insulator layer, the opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

depositing a sleeve insulator layer ~~upon~~ over the top surface of said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

etching the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate, and from the top surface of the upper bulk insulator layer, such that the sleeve insulator layer has a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer~~ adjacent to the top surface of the upper bulk insulator layer, and extends to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the capacitor dielectric layer;

etching the lower bulk insulator layer selective to the sleeve insulator layer to expose the active region on the semiconductor substrate; and

depositing a conductive plug in contact with each of the sleeve insulator layer, the active region on the semiconductor substrate, and a sidewall of the lower bulk insulator layer that is situated in between the contact on the semiconductor substrate and the sleeve insulator layer, wherein the conductive plug has an end comprising a refractory metal silicide, said end of said conductive plug being situated upon the contact on the semiconductor substrate.

8. (currently amended) The method as defined in Claim 7, further comprising:

forming a top insulator layer over the upper bulk insulator layer prior to etching the opening; and

forming an electrically conductive bit line in contact with said conductive plug.

9. (original) The method as defined in Claim 7, wherein the conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

10. (original) The method as defined in Claim 7, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4.

11. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a capacitor storage node thereon, a contact plug on the semiconductor substrate, a lower bulk insulator layer upon the semiconductor substrate, a capacitor dielectric layer upon the lower bulk insulator layer and upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer having a top surface ~~thickness~~ upon the cell plate conductor layer;

~~forming an upper bulk insulator layer having a thickness upon the cell plate insulator layer, wherein said thickness of said upper bulk insulator layer is greater than that of the cell plate insulator layer, said upper bulk insulator layer having a top surface;~~

forming [[a]] an opening defined by the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer, ~~and the upper bulk insulator layer,~~ the opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

forming ~~depositing~~ a sleeve insulator layer upon the top surface of said cell plate insulator layer ~~upper bulk insulator layer~~ and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, and the cell plate conductor layer~~, and the cell plate insulator layer~~;

etching the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate, and from the top surface of the cell plate insulator layer ~~upper bulk insulator layer~~, such that the sleeve insulator layer has a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer~~ adjacent to the top surface of the cell plate insulator layer, and extends to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the capacitor dielectric layer;

forming an upper bulk insulator layer upon the cell plate insulator layer and within the opening adjacent to the sleeve insulator layer;

etching the upper bulk insulator layer and the lower bulk insulator layer to expose the contact plug on the semiconductor substrate; and

depositing an electrically conductive bit line ~~contact~~ extending from the sleeve insulator layer to terminate at the contact plug, the contact plug extending from the electrically conductive bit line ~~contact~~ to ~~the~~ a contact on said semiconductor substrate, wherein the electrically conductive bit line is in contact with the sleeve insulator layer and a sidewall of the lower bulk insulator layer that is situated in between the contact plug and the sleeve insulator layer.

12. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having thereon a capacitor storage node, a transistor on the semiconductor substrate, the transistor having a gate electrode, a lower bulk insulator layer upon the semiconductor substrate and upon the transistor, a capacitor dielectric layer upon the lower bulk insulator layer and upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer;

~~forming an upper bulk insulator layer upon the cell plate insulator layer, said cell plate insulator layer having a thickness that is less than that of the upper bulk insulator layer, said upper bulk insulator layer having a top surface;~~

forming [[a]] an opening defined by the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer, ~~and the upper bulk insulator layer,~~ the opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

forming ~~depositing~~ a sleeve insulator layer upon ~~the~~ a top surface of said cell plate insulator layer ~~upper bulk insulator layer~~ and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, and the cell plate conductor layer~~, and the cell plate insulator layer~~;

etching the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate, and from the top surface of the cell plate insulator layer ~~upper bulk insulator layer~~, such that the sleeve insulator layer has a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer~~ adjacent to the top surface of the cell plate insulator layer, and extends to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the capacitor dielectric layer;

forming an upper bulk insulator layer upon the cell plate insulator layer and within the opening adjacent to the sleeve insulator layer;

etching the upper bulk insulator layer, the lower bulk insulator layer and the transistor to expose the gate electrode; and

depositing an electrically conductive bit line ~~contact~~ extending from the sleeve insulator layer to terminate at the gate electrode, wherein the electrically conductive bit line is in contact with the sleeve insulator layer and a sidewall of the lower bulk insulator layer that is situated in between the gate electrode and the sleeve insulator layer.

13. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer and a capacitor storage node ~~upon~~ thereupon, and further having a capacitor dielectric layer upon the lower bulk insulator layer and on the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer[[:]];

~~forming an upper bulk insulator layer upon the cell plate insulator layer, said upper bulk insulator layer having a top surface and a thickness that is greater than that of said cell plate insulator layer;~~

selectively removing each of ~~the upper bulk insulator layer,~~ the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer to define an opening that terminates at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

forming a sleeve insulator layer upon ~~the~~ a top surface of said cell plate ~~upper bulk~~ insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, and the cell plate conductor layer~~, and the cell plate insulator layer~~;

selectively removing the sleeve insulator layer to have a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer~~ contiguous with the top surface of the cell plate insulator layer, and an extension to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the capacitor dielectric layer; ~~and~~

forming an upper bulk insulator layer upon the cell plate insulator layer and within the opening adjacent to the sleeve insulator layer; and

removing material of the upper bulk insulator layer and the lower bulk insulator layer to expose a contact on the semiconductor substrate.

14. (currently amended) A method according to Claim 13, wherein at least one of selectively removing the sleeve insulator layer and removing material ~~of the lower bulk insulator layer~~ comprises etching.

15. (original) A method according to Claim 13, further comprising forming a conductive plug in contact with each of the sleeve insulator layer, the contact on the semiconductor substrate, and a sidewall of the lower bulk insulator layer that is situated in between the contact on the semiconductor substrate and the sleeve insulator layer.

16. (original) A method according to Claim 15, wherein the conductive plug has an end comprising a refractory metal silicide, said end of said conductive plug being situated upon the contact on the semiconductor substrate.

17. (original) A method as defined in Claim 13, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4..

18. (original) A method as defined in Claim 15, wherein said conductive plug comprises:

a electrically conductive bit line contact extending from the sleeve insulator layer to terminate at a contact plug, the contact plug extending from the electrically conductive bit line contact to the contact on said semiconductor substrate.

19. (original) A method according to Claim 15, wherein the conductive plug comprises at least one electrically conductive material selected from the group consisting of tungsten, titanium/titanium nitride/tungsten, titanium/tungsten, aluminum, copper, a refractory metal silicide with aluminum, and a refractory metal silicide with copper.

20. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer and a capacitor storage node thereupon, and further having, a capacitor dielectric layer upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer ~~storage node~~ and above the lower bulk insulator layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer, the upper bulk insulator layer having a top surface and a thickness that is greater than that of the cell plate insulator layer;

forming an opening that is defined by each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, the cell plate insulator layer, and the upper bulk insulator layer, the opening extending towards the semiconductor substrate and terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

forming a sleeve insulator layer upon said upper bulk insulator layer and within said opening so that the sleeve insulator layer makes contact with each of the lower bulk insulator layer, the cell plate conductor layer, and the cell plate insulator layer;

selectively removing the sleeve insulator layer so as to have a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer~~

contiguous with the top surface of the upper bulk insulator layer, and an extension to an opposite terminus that is within the lower bulk insulator layer and above the semiconductor substrate; and

removing the lower bulk insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate to expose a contact on the semiconductor substrate.

21. (currently amended) The [[A]] method as defined in ~~according to~~ Claim 20, further comprising forming a conductive plug in contact with each of the sleeve insulator layer, the contact on the semiconductor substrate, and a sidewall of the lower bulk insulator layer that is situated in between the contact on the semiconductor substrate and the sleeve insulator layer.

22. (original) The method as defined in Claim 20, further comprising:

forming an electrically conductive plug upon the contact and extending through the sleeve insulator layer.

23. (original) The method as defined in Claim 20, wherein the opposite terminus of the sleeve insulator layer is between the cell dielectric layer and the semiconductor substrate.

24. (original) The method as defined in Claim 22, further comprising:

forming an electrically conductive bit line in contact with said electrically conductive plug.

25. (original) The method as defined in Claim 22, wherein the electrically conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

26. (original) The method as defined in Claim 20, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4.

27. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer and a capacitor storage node thereupon, and further having, a capacitor dielectric layer upon the capacitor storage node and upon the lower bulk insulator layer, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer, wherein the thickness of the upper bulk insulator layer is greater than that of the cell plate insulator layer;

selectively removing each of the upper bulk insulator layer, the cell plate insulator layer, the cell plate conductor layer, the capacitor dielectric layer, and the lower bulk insulator layer so as to form [[a]] an opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

depositing a sleeve insulator layer ~~upon~~ over said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

selectively removing the sleeve insulator layer such that a remaining portion thereof extends from a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer~~ contiguous with a top surface of the upper bulk insulator layer to an opposite terminus within the lower bulk insulator layer and above the semiconductor substrate;

selectively removing the lower bulk insulator layer to create a contact hole defined by the sleeve insulator layer and the lower bulk insulator layer and to expose a contact on the semiconductor substrate; and

forming a conductive plug in the contact hole upon the contact on the semiconductor substrate, said sleeve insulator layer electrically insulating the conductive plug from the cell plate conductor layer.

28. (original) The method as defined in Claim 27, wherein the electrically conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

29. (original) The method as defined in Claim 27, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4..

30. (original) The method as defined in Claim 27, further comprising:

forming an electrically conductive bit line in contact with said electrically conductive plug.

31. (original) The method as defined in Claim 27, wherein the opposite terminus of the sleeve insulator layer is between the cell dielectric layer and the semiconductor substrate.

32. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer and a capacitor storage node thereupon, and further having a capacitor dielectric layer upon the capacitor storage node and upon the lower bulk insulator layer, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer;

selectively removing each of the upper bulk insulator layer, the cell plate insulator layer, the lower bulk insulator layer, the capacitor dielectric layer, and the cell plate conductor layer to define an opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

depositing a sleeve insulator layer ~~upon~~ over said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

selectively removing the sleeve insulator layer such that a remaining portion thereof extends from a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer~~ contiguous with a top surface of the upper bulk insulator layer to an opposite terminus that is within the lower bulk insulator layer and above the semiconductor substrate;

selectively removing material from the lower bulk insulator layer to create a contact hole extending from the upper bulk insulator layer through the sleeve insulator layer and the lower bulk insulator layer to expose a contact on the semiconductor substrate; and

forming a conductive plug in the contact hole upon the contact on the semiconductor substrate and extending to the upper bulk insulator layer, said sleeve insulator layer electrically insulating the conductive plug from the cell plate conductor layer.

33. (original) The method as defined in Claim 32, wherein the conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

34. (original) The method as defined in Claim 32, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4..

35. (original) The method as defined in Claim 32, further comprising:

forming an electrically conductive bit line in contact with said conductive plug.

36. (original) The method as defined in Claim 32, wherein the opposite terminus of the sleeve insulator layer is between the cell dielectric layer and the semiconductor substrate.

37. (currently amended) A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having an active region therein, a capacitor storage node upon the active region, a capacitor dielectric layer upon the capacitor storage node, and a cell plate conductor layer upon the capacitor dielectric layer;

forming a cell plate insulator layer upon the cell plate conductor layer;

forming ~~[[a]]~~ [[a]] an upper bulk insulator layer upon the cell plate insulator layer, wherein the upper bulk insulator layer is greater in thickness than the cell plate insulator layer;

forming a contact hole extending through the upper bulk insulator layer, the cell plate insulator layer, the cell plate conductor layer, the capacitor dielectric layer, and the capacitor storage node to terminate at the active region;

forming a sleeve insulator layer within the contact hole, the sleeve insulator layer extending from a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer and~~ contiguous with a top surface of the upper bulk insulator layer to an opposite terminus that is below the capacitor dielectric layer and above the semiconductor substrate; and

forming an electrically conductive plug extending through the sleeve insulator layer to make contact with the active region and the capacitor storage node, the electrically conductive plug being electrically insulated from the cell plate conductor layer by the sleeve insulator layer.

38. (currently amended) The method as defined in Claim 37, further comprising, prior to forming said electrically conductive plug:

forming a first transistor upon the semiconductor substrate;

forming a second transistor upon the semiconductor substrate[[,]]; and

wherein forming said electrically conductive plug further comprises forming a first portion of the electrically conductive plug so as to be [[is]] situated between the first and second transistors and between the semiconductor substrate and the sleeve insulator layer.

39. (original) The method as defined in Claim 38, wherein the first portion of the electrically conductive plug is enclosed within the sleeve insulator layer.

40. (original) The method as defined in Claim 37, wherein the electrically conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

41. (original) The method as defined in Claim 37, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4.

42. (original) The method as defined in Claim 37, further comprising:

forming an electrically conductive bit line in contact with said electrically conductive plug.

43. (currently amended) A method of fabricating an integrated circuit that includes a semiconductor substrate having an active region therein, a capacitor storage node upon the active region, a capacitor dielectric layer upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer, ~~and an upper bulk insulator layer upon the cell plate insulator layer,~~ the method comprising:

forming a contact hole extending through ~~the upper bulk insulator layer,~~ the cell plate insulator layer, the cell plate conductor layer, the capacitor dielectric layer, and the capacitor storage node to terminate at the active region;

forming a sleeve insulator layer within the contact hole, the sleeve insulator layer extending from a terminus ~~at an interface between the upper bulk insulator layer and the cell plate insulator layer and~~ adjacent to the cell plate insulator layer to an opposite terminus that is below the capacitor dielectric layer and above the semiconductor substrate; and

forming an electrically conductive plug extending through the sleeve insulator layer to make contact with the active region and the capacitor storage node, the electrically conductive plug being electrically insulated from the cell plate conductor layer by the sleeve insulator layer.

REMARKS

Claims 1, 6, 7, 8, 11-14, 20, 21, 27, 32, 37, 38, and 43 have been amended, and claims 1-43 are pending in the present application. The claim amendments are supported by the specification and drawings as originally filed, with no new matter being added. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

The specification has been amended to correct typographical or grammatical errors. Claims 1, 6, 7, 8, 11-14, 20, 21, 27, 32, 37, 38, and 43 have been amended to correct typographical or grammatical errors, or for clarity, and not for reasons related to patentability. Applicants note that original claims 1-43 were previously allowed.

In view of the foregoing, Applicants respectfully request allowance of the present claims. In the event there is any impediment to allowance of the claims, which could be clarified in a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 22nd day of September 2003.

Respectfully submitted,

Gregory M. Taylor
Attorney for Applicants
Registration No. 34,263
Customer No. 022901

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